Team Name: sdmay24-40
Team Members: Huyen Vy Pham, Aaron McCarville, Gunnar Hageman, Benjamin Podjenski, Noah Gaffney
Report Period: Aug 28-Sept 10

Summary of Progress in this Period

The team talked to advisor and client (professor Al Qaseer) to understand the requirements of the project.
The team has drafted a rough timeline for the project.
Each team member has been assigned with a role in the project.
The FPGA is decided.
The simulation for the PLL filter circuit is completed.
Radar Eval board schematic is completed.

Pending Issues

We must decide on an ADC.
We need to check that the Achitry AU has enough pins for our design.
We need to discuss more on the software part of the project.

Plans for Upcoming Reporting Period

Finish schematic/layout review Radar eval board.
Order Radar eval board.
Decided on the loop bandwidth of the PLL.
Start working on the software and the FPGA programing.